AMENDMENTS TO THE SPECIFICATION

IN THE SPECIFICATION:

Page 1:

After the title, insert the following paragraph:

CROSS-REFERENCE TO RELATED APPLICATION

This application is a division of Application No. 10/166,145 filed June 11, 2002.

Page 1:

Please substitute the following paragraph for the paragraph beginning at line 10:

Of electrically programmable nonvolatile semiconductor memory devices, a bulk erasable memory or so-called flash memory is known. Flash memories provide excellent portability and shock ~~proof~~ resistance and are electrically bulk erasable. ~~From~~ For these reasons, demands for flash memories as storage devices of compact portable information apparatuses such as portable personal computers and digital still cameras are rapidly increasing. Reduction in a bit cost by a smaller memory cell area is an important factor for market expansion. Various memory cells realizing this have been proposed, for example, as described in " Ohyo

Butsuri (or Applied Physics)", Vol. 65, No. 11, pp. 1114 - 1124 published by the Japan Society of Applied Physics on November 10, 1996 (hereinafter called "Document 1").

Page 1:

Please substitute the following paragraph for the paragraph beginning at line 26:

A virtual ground type memory cell utilizing a three-layer polysilicon gate is described, for example, in JP-B-2694618 (registered on September 12, 1997) corresponding to U.S. Patent 5,095,344. This memory cell is constituted of semiconductor regions formed in a well of a semiconductor substrate and three gates. The three gates include a control gate formed on the well and an erase gate formed between the control gate and a floating gate disposed near each other. These three gates are made of polysilicon and are separated by insulator films. The floating gate and well are also separated by an insulator film. The control gate extending in the row direction constitutes a word line. The source/drain diffusion regions are formed along the column direction and are of a virtual ground type that shares the diffusion regions with adjacent memory cells. With this layout, a pitch in the row direction can be ~~relaxed~~reduced. The erase gate is parallel to the channel

and disposed between and in parallel to the word lines (control gates). In writing data in a memory cell described in Document 1, independent positive voltages are applied to the word line and drain, and 0 V is applied to the well, source and erase gate. Hot electrons are therefore generated in the channel region near the drain so that electrons are injected into the floating gate and the threshold voltage of the memory cell rises. In erasing data in the memory cell, a positive voltage is applied to the erase gate, and 0 V is applied to the word line, source, drain and well. Electrons are drained from the floating gate into the erase gate so that the threshold voltage lowers.

Page 3:

Please substitute the following paragraph for the paragraph beginning at line 26:

The breakdown voltage between the diffusion layer and well is always required to be about 5V or higher during the write operation ~~from~~ for the following reason.

Page 4:

Please substitute the following paragraph for the paragraph beginning at line 11:

In the cell of the type that data is written by Fowler-Nordheim tunneling electron injection into the whole channel region, for example, about 18 V is applied to the control gate above the floating gate and 0 V is applied to the source/drain to write data by a tunnel current from the inversion layer to the floating gate. In this case, it is necessary to inhibit data write to other cells of the memory array having the same control gate. To this end, for example, about 5 V or higher is applied to the drains of the data write inhibited cells to float the sources so that the inversion channels having the same potential as the drains can be formed under the floating gates. In this manner, the potential difference between the floating gate and well can be ~~relaxed~~ reduced and electron tunneling from the channel to the floating gate can be prevented. In this case, the breakdown voltage between the diffusion layer and well is required to be the drain voltage or higher.

Page 8:

Please substitute the following paragraph for the paragraph beginning at line 26:

According to another embodiment, a ~~manufacture~~ manufacturing method for a nonvolatile semiconductor memory

device is provided which comprises: a step of forming a well of a first conductivity type in a semiconductor substrate; a step of forming a pair of semiconductor regions of a second conductivity type formed in the well of the first conductivity type, the pair of semiconductor regions being used as a source and a drain; a step of forming a first gate on the semiconductor substrate via a first gate insulator; a step of forming a second gate on a second insulator film covering the first gate; and a step of forming an impurity doped region of the first conductivity type having an impurity concentration higher than the well in a channel region between the pair of semiconductor regions, the impurity doped region being not in contact with the semiconductor regions. The semiconductor regions and the impurity region are formed in a self-alignment manner by tilted ion implantation tilted in opposite directions from a normal of the semiconductor substrate, by using the first gate as a mask.

Page 9:

Please substitute the following paragraph for the paragraph beginning at line 23:

According to another embodiment of the invention, a ~~manufacture~~ manufacturing method for a nonvolatile semiconductor memory device, is provided which comprises: a step of forming dummy gates on a semiconductor substrate having a first ~~conductive~~ conductivity type region on a surface thereof; a step of forming a pair of source/drain diffusion layers of a second conductivity type in a surface layer of the semiconductor substrate between adjacent dummy gates, by using the dummy gates as a mask; a step of burying the dummy gates with a first insulator film; a step of removing a portion of the first insulator film to expose an upper surface of each dummy ~~gates~~ gate without exposing the surface of the semiconductor substrate; a step of removing the dummy gates; a step of depositing a silicon nitride film or a polysilicon film on an upper surface of the first insulator film and an inner surface of a groove formed in the first insulator film by removing each dummy gate, to the extent that the groove is not completely buried; a step of etching back the silicon nitride film or the polysilicon film to form side walls on an inner surface of each groove; and a step of implanting impurities of the first conductivity type to form a heavily impurity doped region having an impurity concentration higher than the

first conductivity type region in the surface layer of the semiconductor substrate between the pair of source/drain diffusion ~~lagers~~layers, by using the first insulator film and the side walls as a mask.

Page 16:

Please substitute the following paragraph for the paragraph beginning at line 23:

The control gate (second gate) 211a of each memory cell extends in the row direction (x-direction) and constitutes the word line WL. The floating gate (first gate) 203b and well 201 are separated by a gate insulator film (first insulator film) 202, the floating gate 203b and third gate 207a are separated by an insulator film (third insulator film) 206a, the floating gate 203b and word line (control gate) 211a are separated by an insulator film (second insulator film) 210, and the third gate 207a and word line 211a are separated by an insulator film (fourth insulator film) 208a.

Page 19:

Please substitute the following paragraph for the paragraph beginning at line 25:

~~From~~ For the above reasons, it is essential to prevent punch-through both under the first and third gates. Since the region 501 is formed extending under both the first and third gates, it is possible to prevent punch-through.

Page 20:

Please substitute the following paragraph for the paragraph beginning at line 2:

In this embodiment, the ~~first~~ third gate may be used as an erase gate for draining electrons from an adjacent floating gate when data is erased.

Page 20:

Please substitute the following paragraph for the paragraph beginning at line 15:

Next, a polysilicon film 207 doped with ~~phosphor~~ phosphorus (P) to be used as a third gate 207a and a silicon oxide film 208 are sequentially deposited (Fig. 3B). For example, chemical vapor deposition (CVD) is performed for depositing the polysilicon film 207 and silicon oxide film 208.

Page 22:

Please substitute the following paragraph for the paragraph beginning at line 28:

Next, a silicon oxide film 206 is formed for separating the third gate 207a and floating gate 203b. This silicon oxide film is formed through thermal oxidation

of the polysilicon film 207a, through CVD or through a combination of both the thermal oxidation and CVD (Fig. 4C).

Page 23:

Please substitute the following paragraph for the paragraph beginning at line 6:

Thereafter, a polysilicon film 203 doped with ~~phosphorous~~ phosphorus (P) to be used as the floating gate 203b is deposited to the extent that a groove of the polysilicon film 203 between the third gate patterns 207a is not completely filled with polysilicon (Fig. 5A).

Page 23:

Please substitute the following paragraph for the paragraph beginning at line 12:

Next, photoresist 213 is coated, filling the groove (Fig. 5B), and the photoresist and polysilicon film 203 are etched back to pattern the polysilicon film 203 to be used as the floating gate.

Page 24:

Please substitute the following paragraph for the paragraph beginning at line 2:

Although not shown, after an interlayer insulating film is formed, contact holes are formed reaching the word line 211a, source/drain diffusion layers 205, well 201 and third gate ~~203a~~207a. A metal film is thereafter deposited and patterned to form metal wires and complete memory cells.

Page 25:

Please substitute the following paragraph for the paragraph beginning at line 10:

In writing data, i.e., in injecting electrons from the well into the floating gate, a voltage of about 5 V is applied to the diffusion layer of write inhibited cells on the word line to ~~relax~~ reduce the potential difference from that of the inversion channel under the floating gate and prevent electrons from being injected from the well into the floating gate.

Page 27:

Please substitute the following paragraph for the paragraph beginning at line 28:

Next, the side walls 309a or deposited film 309 are removed, for example, by wet etching or isotropic dry

etching. Thereafter, a polysilicon film 310 doped with ~~phosphor~~ phosphorus to be used as the floating gate is formed completely filling the gap (Fig. 12A). The polysilicon film 310 is removed until the oxide film pattern 308b is exposed by chemical mechanical polishing or etch-back (Fig. 12B). Next, a polysilicon film 311 doped with ~~phosphorous~~ phosphorus is deposited (Fig. 12C).

Page 29:

Please substitute the following paragraph for the paragraph beginning at line 10:

In the second embodiment, after the polysilicon film 310 doped with ~~phosphorous~~ phosphorus to be used as the floating gate is deposited completely filling the gap (Fig. 12A), the polysilicon film 310 is worked by a chemical mechanical polishing method or etch-back until the oxide film pattern 308b is exposed. Thereafter, the polysilicon film 311 doped with ~~phosphorous~~ phosphorus is deposited and patterned. In the third embodiment, the polysilicon film 310 is patterned.

Page 31:

Please substitute the following paragraph for the paragraph beginning at line 25:

By using processes similar to those of the second to fourth embodiments, the heavily impurity doped regions 306 are formed (Fig. 10C or Fig. 11), the side wall 309a, or deposited silicon nitride film or polysilicon film 309 is removed by wet etching or isotropic dry etching. Thereafter, a polysilicon film doped with ~~phosphorous~~ phosphorus to be used as the floating gate is deposited to the extent that the gap is not completely filled (Fig. 16A). The polysilicon film 310 to be used as the floating gate is worked by photoresist coating and etch-back similar to the first embodiment (Fig. 16B). The floating gate may be formed by a chemical mechanical polishing method.

Page 34:

Please substitute the following paragraph for the paragraph beginning at line 12:

If the polysilicon film doped with ~~phosphorous~~ phosphorus to be used as the floating gate is deposited to the extent that the gap is not completely filled as in the fifth and sixth embodiments, the heavily impurity doped region 306 may be formed by positively utilizing the recess of the polysilicon film.

Page 34:

Please substitute the following paragraph for the paragraph beginning at line 19:

After the process of the second embodiment shown in Fig. 9C, a polysilicon film 310 doped with ~~phosphorous~~ phosphorus to be used as the floating gate is deposited to the extent that the gap is not completely filled (Fig. 18A). Then, boron or boron fluoride ions are implanted vertically through the recess to form heavily impurity doped regions (Fig. 18B).

Page 36:

Please substitute the following paragraph for the paragraph beginning at line 22:

As shown in Fig. 21B, the floating gate 404b and control gate 409a are formed on the well. Near ~~at~~ the boundary between the floating gate and one control gate, a source/drain layer 405 is formed, and near ~~at~~ the boundary between the floating gate and another control gate, a heavily impurity doped region 500 is formed. The source/drain diffusion layers extend in the y-direction and function as a local bit line and a local source line of each memory cell. The memory cell of this embodiment is a virtual ground type that shares the source/drain diffusion regions with adjacent memory cells.

Page 42:

Please substitute the following paragraph for the paragraph beginning at line 4:

It should be further understood by those skilled in the art that although the foregoing description has been made ~~on~~ with respect to preferred embodiments of the invention, the invention is not limited thereto and various changes and modifications may be made without departing from the spirit of the invention and the scope of the appended claims.